Project 9
Common Emitter Amplifier
(designed for two lab periods)

Objective: This project will show how the h-parameters for a BJT can be measured and used in an equivalent circuit model for the BJT. A CE small signal amplifier will be biased and designed to specifications along with both low and high frequency response and adjustment. Series-series feedback will also be used to control the bandwidth and input impedance of the CE amplifier.

Components: 2N2222 BJT

Introduction:

In order for circuits involving transistors to be analyzed, the terminal behavior of the transistor must be characterized by a model. Two of the models often used for a BJT are the hybrid-π and the h-parameter models. The complete hybrid-π circuit model for the BJT is shown in Figure 9-1. This model includes the internal capacitances and output resistance of the BJT. Inclusion of the internal transistor capacitances makes the hybrid-π model valid throughout the entire frequency range of the transistor. Typical data sheet values of C_π and C_μ are 13 pF and 8 pF respectively. These values are so small that C_π and C_μ may be considered open circuits for midband frequencies. The resistance r_x typically has a value in the tens of ohms and can be considered a short circuit while r_μ and r_o are usually extremely large in value and can be considered open circuits.

The h-parameter small signal model for the BJT is characterized by the four h-parameters and is shown in Figure 9-2. Unlike the hybrid-π model, the h-parameter model does not ordinarily include frequency related effects and components and is therefore generally valid only at midband frequencies and below . However the h-parameter model is very useful since the h-parameters can be easily measured for a BJT. The value of h_{re} is usually on the order of 10^{-4} and can be considered a short circuit. The value of h_{oe} is usually on the order of 10^{-5} S making $1/h_{oe}$ effectively an open circuit for most circuit configurations and biases. Making the same assumptions, the hybrid-π and h-parameter models are equivalent at midband frequencies.

For a transistor to operate as an amplifier, it must have a stable bias in the active region. To bias a transistor, a constant DC current must be established in the collector and emitter. This current should be as insensitive as possible to variations in temperature and β (or h_{fe}). The voltage across the base-emitter junction decreases about 2 mV for each 1 °C rise in temperature, therefore it is important to stabilize V_{BE} to ensure that the transistor does not overheat. The circuit shown in Figure 9-3 is the biasing scheme most often used for discrete transistor circuits. For this circuit, the base is supplied with a fraction of the supply voltage V_{CC} through the voltage divider R_{B1}, R_{B2}. For ease of circuit analysis, the Thevenin equivalent circuit shown in Figure 9-4 can replace the voltage divider network. To ensure that the emitter current is insensitive to variations in β and V_{BE}, V_{BB} should be much greater than V_{BE} and R_{BB} should be much less than βR_E. R_{BB} is usually 20-30% of the product βR_E. The voltage across R_E is also usually 2-3 volts for good β stabilization. This same biasing scheme can be used for all three of the BJT amplifier configurations (CB, CC, CE).

The BJT CE amplifier is shown in Figure 9-5. The signal source and resistive load are capacitively coupled to the amplifier. The coupling capacitors C_1 and C_2, emitter bypass capacitor C_E, and internal transistor capacitances shape the frequency response of the amplifier. A typical amplifier frequency response curve is shown in Figure 9-6. The low half power corner frequency F_L is controlled by the input and output coupling capacitors and the emitter bypass capacitor. The high half power corner frequency F_H is controlled by the internal transistor capacitances and any separate load capacitor. The bandwidth is the difference between the high and low corner frequencies (F_H - F_L). As the signal frequency drops below midband, the impedance of the coupling capacitors C_1 and C_2 and emitter bypass capacitor C_E increases. The coupling capacitors drop more signal voltage and the emitter bypass capacitor begins to open up and causes increased series-series feedback resulting in a reduction of the gain. One method of relating C_1, C_2, and C_E to the low cutoff frequency is the short circuit time constant method. The time constant method is advantageous because it provides an approximate value for the cutoff frequencies without exactly finding all the poles and zeros of a circuit. The time constant method also helps show which capacitors are dominant in determining the corner frequencies. The short circuit time constant method relates F_L and circuit capacitors by:

$$F_L \approx \frac{1}{2\pi} \sum_{i=1}^{n_c} \frac{1}{C_i R_{is}}$$

where F_L is the low half power frequency, n_c is the number of coupling and bypass capacitors in the circuit, and C_i is the value, in Farads, of the ith capacitor. R_{is} is the resistance facing the ith capacitor with the ith capacitor removed and all other coupling and bypass capacitors replaced by short circuits and the input signal reduced to zero. This resistance calculation is repeated for each coupling and bypass capacitor in the circuit.

The internal capacitances of a transistor have values in the picofarad (pF) range that begin to decrease the gain of the amplifier for frequencies above midband. A method of relating the internal transistor capacitances C_π and C_m to the high cutoff frequency is the open circuit time constant method. This method relates F_H and the internal transistor capacitances by:

$$F_H \approx \frac{1}{2\pi} \sum_{i=1}^{n_c} \frac{1}{C_i R_{io}}$$

where F_H is the high half power frequency, n_c is the number of internal transistor capacitors in the circuit, and C_i is the value, in Farads, of the ith capacitor. R_{io} is the resistance facing the ith capacitor with the ith capacitor removed and all internal transistor capacitors replaced by open circuits and the input signal reduced to zero. This resistance calculation is repeated for each internal transistor capacitor in the circuit.

When the emitter resistor of the CE amplifier is left unbypassed, the input current signal flows through the unbypassed emitter resistor as does the output signal current. This unbypassed emitter resistor in the CE amplifier produces series-series feedback. The feedback resistor is R_E. Feedback is used in amplifiers to control input and output impedances, extend bandwidth, enhance signal-to-noise ratio, and reduce parameter sensitivity. These feedback performance improvements are all at the expense of gain in the amplifier.

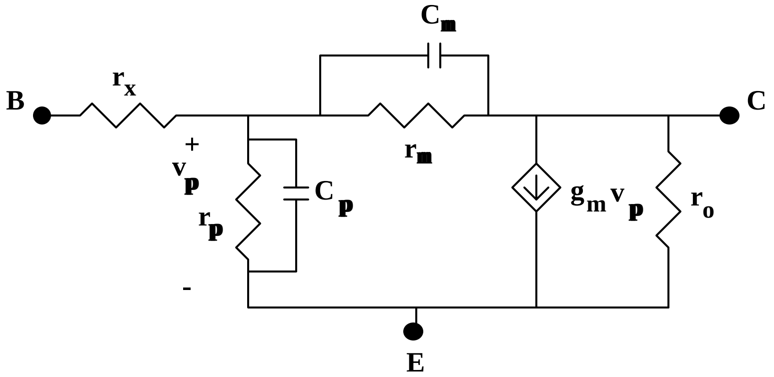

Figure 9 - 1: Hybrid-π BJT Model

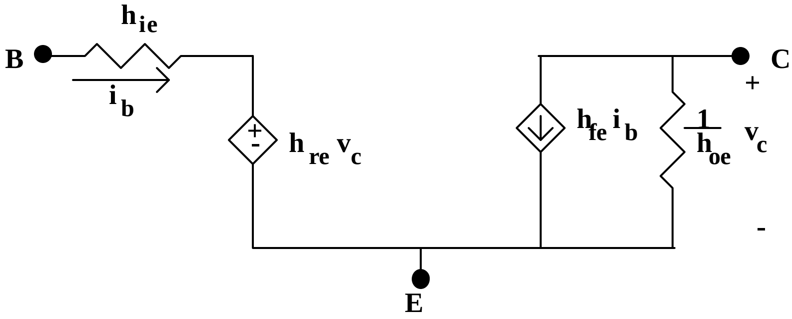

Figure 9 - 2: h Parameter BJT Model

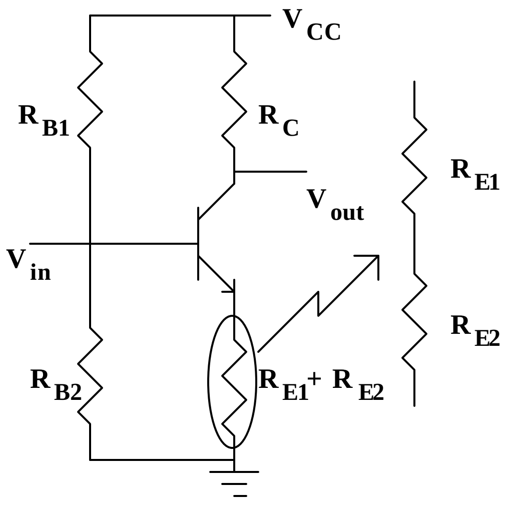

Figure 9 - 3: BJT Typical Biasing Circuit

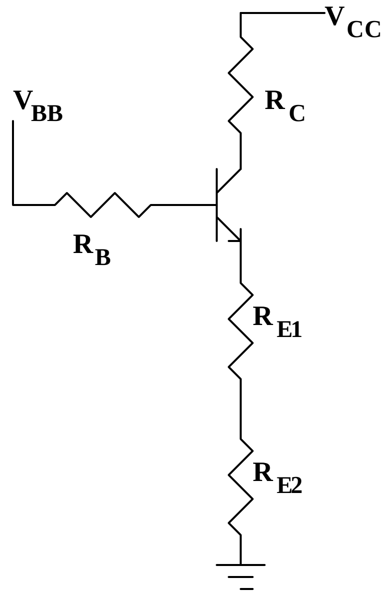

Figure 9 - 4: Thevenin Equivalent Biasing Circuit

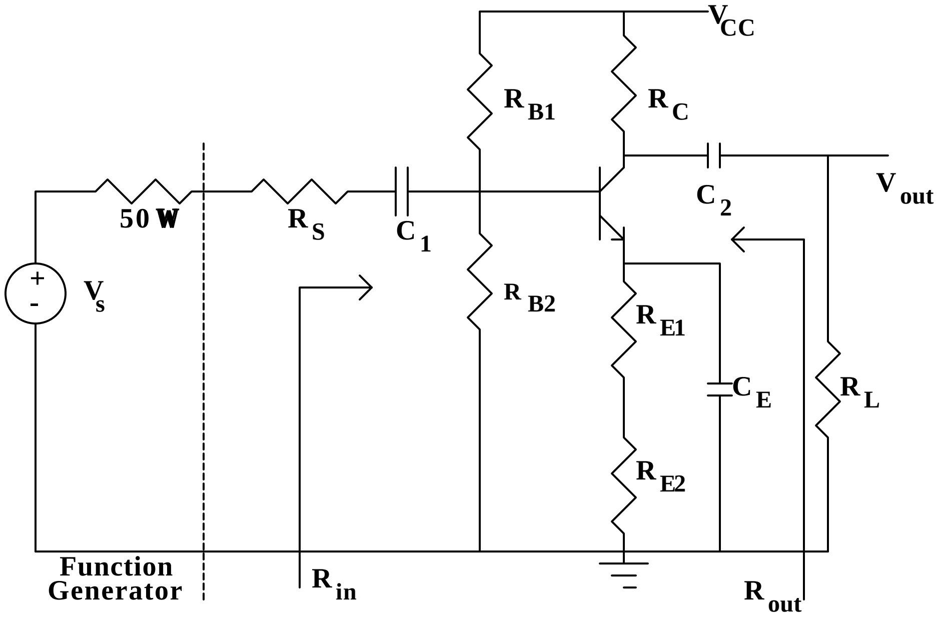

Figure 9 - 5: Common Emitter Amplifier

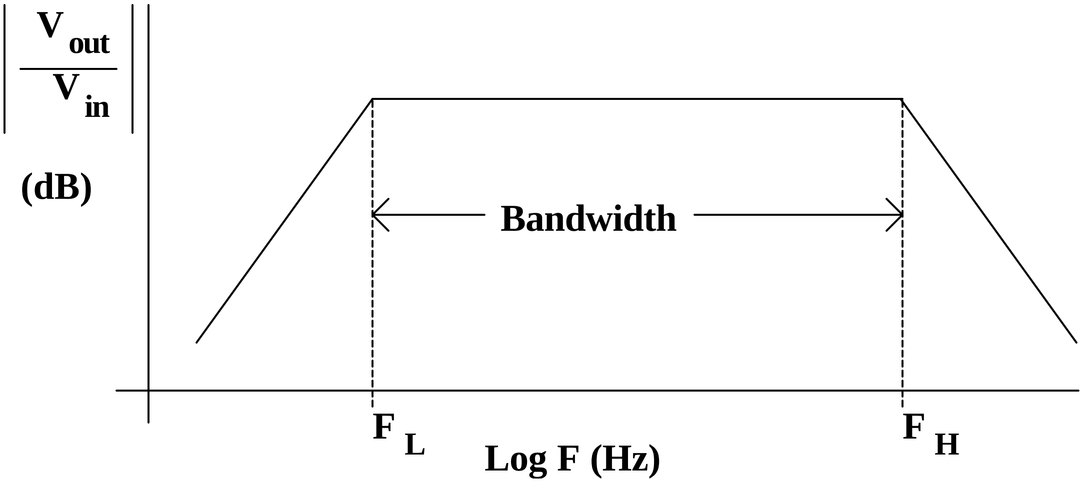

Figure 9 - 6: Typical Amplifier Frequency Bode Diagram

Design:

Design a common emitter amplifier with R_E $[R_{E1} + R_{E2}]$ completely bypassed with the following specifications:

1. use a 2N2222 BJT and a 12 volt DC supply
2. midband gain $V_O/V_S \geq 50$
3. low cutoff frequency F_L between 100 Hz and 200 Hz
4. input impedance as seen by the source ≥ 1 kΩ
5. V_O symmetric swing ≥ 2.0 volts peak (4 V p-p)
6. load resistor R_L = 1.5 kΩ
7. source resistance R_S = 50 Ω (this is in addition to the function generator's internal resistance)

Lab Procedure: (steps 1 and 2 may be omitted if done prior to this lab period and the same BJT is used)

1. From the digital curve tracer, find the value of β_{DC} and β_{AC} at the designed Q-point of the CE amplifier. Remember $\beta_{DC} = I_C/I_B$ and $\beta_{AC} = \Delta I_C/\Delta I_B$. How do the two β values compare?
2. Determine the values of h_{oe} and h_{ie} from the digital curve tracer. The slope of the transistor I_C-V_{CE} curves in the active region is h_{oe}. Find h_{ie} by looking at the base-emitter junction as a diode on the curve tracer. The tangent slope of the I_B-V_{BE} curve at the I_{BQ} point is $1/h_{ie}$.

3. Construct the CE amplifier of Figure 9-5. Remember R_S is installed in addition to the internal 50 Ω resistance of the function generator. Note that (R_{E1} + R_{E2}) should equal the designed value for R_E and $R_{E1} \approx R_{E2}$. Verify that the specifications have been met by measuring the Q-point, midband voltage gain, and peak symmetric output voltage swing. Note any distortion in the output signal.
4. Observe the loading affect by replacing R_L first by 150 Ω and then by 15 kΩ. Note any changes in the output signal and comment on the loading affect.
5. Use computer control to record and plot the frequency response. Find the corner frequencies and bandwidth to verify that the specifications have been met.
6. Measure the input impedance seen by the source [look at the current through R_S and the node voltage on the transistor side of R_S] and the output impedance seen by the load resistor [look at the open circuit voltage and the current through and voltage across R_L = 1.5 kΩ]. Verify that the input impedance specification has been met.
7. Now adjust the bypass capacitor C_E so that R_{E1} is not bypassed (which is a series-series feedback configuration). Measure the Q-point and midband voltage gain. Note any distortion in the output signal.
8. Repeat steps 4 - 6.
9. Remove the bypass capacitor C_E completely. Measure the Q-point and midband voltage gain. Note any distortion in the output signal.
10. Repeat steps 4 - 6.

Questions:

1. Compare the measurements in Lab Procedures 3-10 to the theoretical predictions such as those obtained using PSPICE®. Note how increasing the feedback affects the gain, bandwidth, and input and output impedances.
2. Can you think of a way to vary the amount of feedback (gain) using a potentiometer of a value equal to R_E without affecting the Q point?
3. How can F_H be reduced using external components?
4. Why is the value of F_H measured in the lab generally different from (lower than) the value of F_H determined using PSPICE® or manual calculations?